Amendments to the Claims

Kindly amend claims 1-4, 6, 9, 11, 14, 17-19, 22 & 23 as set forth below. In compliance with the Revised Amendment Format, a complete listing of claims is provided herein. The changes in the amended claims are shown by strikethrough (for deleted matter) and underlining (for added matter).

1. (Currently Amended) A built-in self test circuit for testing a clock and data recovery circuit comprising:

data generating means for generating ~~a test data byte~~ test data, wherein the test data comprises a frame header;

serializing means coupled to the data generating means for converting the test data ~~byte~~ into serial test data;

clock and data recovery means coupled to the output of the serializing means for recovering the clock and test data from the serial test data;

deserializing means coupled to the output of the clock and data recovery means for converting the recovered serial test data into recovered test data ~~a recovered test data byte~~; and

analyzing means connected to the output of the deserializing means for comparing a beginning portion of the recovered test data ~~byte~~ to the frame header, ~~test data byte~~

wherein a match between the beginning portion of the recovered test data and the frame header indicates a positive outcome of said testing.

2. (Currently Amended) The circuit of claim 1 wherein said clock and data recovery means ~~circuit~~ comprises a phase lock loop.

3. (Currently Amended) The circuit of claim 2 further comprising a multiplexer coupled to the clock and data recovery means ~~circuit~~ for inputting operational serial data or said serial test data upon setting of a data selection signal (B-ENB).

4. (Currently Amended) The circuit of claim 2 further comprising a first multiplexer coupled to the serializing means for inputting operational parallel data ~~byte~~ or said test data ~~byte~~ upon setting of a data selection signal (B-ENB).

5. (Original) The circuit of claim 4 further comprising a second multiplexer coupled to the clock and data recovery circuit for inputting operational serial data or said serial test data upon setting of a data selection signal (B-ENB).

6. (Currently Amended) The circuit of claim 5 wherein said test data ~~byte~~ is in the form of a SONET frame, and said analyzing means comprises means for detecting the start of a SONET frame.

7. (Original) The circuit of claim 6 further comprising a state machine to control said generating means and said analyzing means.

8. (Original) The circuit of claim 7 wherein said data generating means is a programmable data generator.

9. (Currently Amended) The circuit of claim 1 further comprising a multiplexer coupled to the serializing means for inputting operational parallel data ~~byte~~ or said test data ~~byte~~ upon setting of a data selection signal (B-ENB).

10. (Original) The circuit of claim 1 further comprising a multiplexer coupled to the clock and data recovery circuit for inputting operational serial data or said serial test data upon setting of a data selection signal (B-ENB).

11. (Currently Amended) The circuit of claim 1 wherein said test data ~~byte~~ is in the form of a SONET frame, and said analyzing means comprises means for detecting the start of a SONET frame.

12. (Original) The circuit of claim 1 further comprising a state machine to control said generating means and said analyzing means.

13. (Original) The circuit of claim 1 wherein said data generating means is a programmable data generator.

14. (Currently Amended) A method for testing a clock and data recovery circuit comprising:

generating ~~an~~ initial test data ~~byte~~, wherein the initial test data comprises a frame header;

inputting the initial test data ~~byte~~ to a serializer for conversion into serial test data;

sending the serial test data to the clock and data recovery circuit for recovering the clock and test data from the serial test data;

inputting the recovered serial test data to a deserializer for conversion into recovered test data ~~a recovered test data byte~~; and

comparing a beginning portion of the recovered test data ~~byte~~ to the frame header ~~initial test data byte~~,

wherein a match between the beginning portion of the recovered test data and the frame header indicates a positive outcome of said testing.

15. (Original) The method of claim 14 wherein said clock and data recovery circuit comprises a phase lock loop.

16. (Original) The method of claim 15 further comprising an initial step of waiting for a predetermined period of time to allow said phase lock loop to lock to a predetermined frequency before beginning of said generating.

17. (Currently Amended) The method of claim 16 further comprising:

generating new test data ~~a new test data byte~~; and

repeating said serializing, recovering, deserializing and comparing ~~analyzing~~ until the beginning portion of the recovered test data ~~byte~~ matches the frame header ~~test data byte~~.

18. (Currently Amended) The method of claim 17 wherein said generating new test data ~~a new test data byte~~ and said repeating are performed until a counter reaches a predetermined number of pulses.

19. (Currently Amended) The method of claim 18 wherein said generating and said comparing ~~analyzing~~ are controlled by a state machine.

20. (Original) The method of claim 19 wherein said counter is included within said state machine.

21. (Original) The method of claim 14 further comprising an initial step of waiting for a predetermined period of time to allow said phase lock loop to lock to a predetermined frequency before beginning of said generating.

22. (Currently Amended) The method of claim 14 further comprising:

generating new test data ~~a new test data byte~~; and

repeating said serializing, recovering, deserializing and comparing ~~analyzing~~ until the beginning portion of the recovered test data ~~byte~~ matches the frame header ~~test data byte~~.

23. (Currently Amended) The method of claim 14 wherein said generating and said comparing ~~analyzing~~ are controlled by a state machine.

24. (New) A built-in self test circuit for testing a clock and data recovery circuit comprising:

data generating means for generating a test data byte;

serializing means coupled to the data generating means for converting the test data byte into serial test data;

clock and data recovery means coupled to the output of the serializing means for recovering the clock and test data from the serial test data;

deserializing means coupled to the output of the clock and data recovery means for converting the recovered serial test data into a recovered test data byte; and

analyzing means connected to the output of the deserializing means for comparing the recovered test data byte to the test data byte,

wherein an outcome of said testing comprises indicating improper operation of the clock and data recovery means.

25. (New) The circuit of claim 24 wherein said clock and data recovery means comprises a phase lock loop.

26. (New) The circuit of claim 25 further comprising a multiplexer coupled to the clock and data recovery means for inputting operational serial data or said serial test data upon setting of a data selection signal (B-ENB).

27. (New) The circuit of claim 25 further comprising a first multiplexer coupled to the serializing means for inputting operational data byte or said test data byte upon setting of a data selection signal (B-ENB).

28. (New) The circuit of claim 27 further comprising a second multiplexer coupled to the clock and data recovery circuit for inputting operational serial data or said serial test data upon setting of a data selection signal (B-ENB).

29. (New) The circuit of claim 28 wherein said test data byte is in the form of a SONET frame, and said analyzing means comprises means for detecting the start of a SONET frame.

30. (New) The circuit of claim 29 further comprising a state machine to control said generating means and said analyzing means.

31. (New) The circuit of claim 30 wherein said data generating means is a programmable data generator.

32. (New) The circuit of claim 24 further comprising a multiplexer coupled to the serializing means for inputting operational data byte or said test data byte upon setting of a data selection signal (B-ENB).

33. (New) The circuit of claim 24 further comprising a multiplexer coupled to the clock and data recovery circuit for inputting operational serial data or said serial test data upon setting of a data selection signal (B-ENB).

34. (New) The circuit of claim 24 wherein said test data byte is in the form of a SONET frame, and said analyzing means comprises means for detecting the start of a SONET frame.

35. (New) The circuit of claim 24 further comprising a state machine to control said generating means and said analyzing means.

36. (New) The circuit of claim 24 wherein said data generating means is a programmable data generator.